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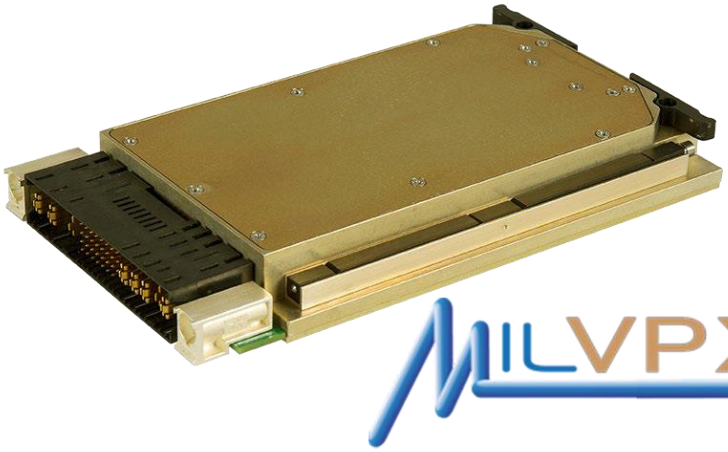
M4065 SERIES

VITA 62 Compliant 3U VPX
700W



OVERVIEW

MilPower 700W VPX Power Supply

- **DC-DC Converter**
- **VITA 62 Compliant, 3U form factor**
- **600W (–55°C to +85°C), 700W peak[1]**
- **6 Outputs**
- **Efficiency up to 88% (86% Typical at Full Load)**
- **Fully Operating: –55°C to +85°C (measured at unit edge)**
- **Designed to meet: MIL-STD-454, MIL-STD-461, MIL-STD-704, MIL-STD-1275, MIL-STD-810**

***Contact Factory for more details**

SPECIAL FEATURES

- VITA 62 compliant
- Wide input range
- Remote sense
- Fixed switching frequency(250khz)
- External synchronization capability
- Current sharing for VS1, VS2, VS3 - Optional
- Indefinite short circuit Protection
- Over-voltage shutdown with auto-recovery
- Reverse battery protection
- Over temperature shutdown with auto-recovery
- EMI filters included
- IPMI communication

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Electrical Specifications

DC Input
18 to 48 V_{DC}

Full compliance for MS-704 50V surge, No damage MS-1275 & MS-704A

Can be configured for continuous work during 100V surge, 12V surges IAW MIL-STD-1275E

DC Output

VS1:	12V	up to 30A
VS2:	3.3V	up to 20A
VS3:	5V	up to 30A
12V_Aux:	12V	up to 1A
-12V_Aux:	-12V	up to 1A
3.3V_Aux:	3.3V	up to 5A

Peak power option:

VS1:	12V	up to 40A
VS3:	5V	up to 35A

Current Sharing
Optional for VS1, VS2, VS3

Isolation
Over 20 MΩ at test voltage:
200V between Input and Output
200V between Input and Case
100V between Output and Case

Line/Load regulation
See Table 2 on page 7

Efficiency
Up to 87 %
(86.1% at Full load room temperature)

EMC
Complies with MIL-STD-461F[1] [2] (5µH LISN[2]): CE101, CE102, CS101, CS114, CS115, CS116

Ripple and Noise
Typically less than 50mV_{p-p} (max.1%$_p$). Measured across a 0.1µF capacitor and 10µF capacitor on load at Input Voltage of 18V-36V, all Temperature Range.

Load Transient Overshoot and Undershoot
Output dynamic response of less than5% at load Step of 30%-90%.
Output returns to regulation in less than 1mSec

Communication
IPMI protocol available for voltages, currents and temperature for all positive voltages (GAx, SCL, SDA)

Notes:
1. Compliance achieved with 5µH LISN, shielded cable and static resistive load.
2. M4165 for 50 µH compliance

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Environmental [1]
Design to Meet MIL-STD-810G

Temperature
Operating: –55°C to +85°C
at unit edge
Storage: –55°C to +125°C

Altitude
Method 500.5, Procedure I & II
Storage/Air Transport: 40 Kft
Operation/Air carriage: 70 Kft

Salt Fog:
Method 509.5

Fungus
Does not support fungus growth, in accordance with the guidelines of MIL-STD-454, Requirement 4.

Humidity
Method 507.5, Up to 95% RH

Shock
Method 516.6
40g, 11msec saw-tooth (all directions)

Vibration
Shock: Saw-tooth, 20g peak, 11mS.
Vibration: Figure 514.6E-1. General minimum integrity exposure. (1 hour per axis.)

Note 1: ***Environmental Stress Screening (ESS)*** Including random vibration and thermal cycles is also available. **Please consult factory for details.**

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Protections [1]

Input

- **Input Reverse Polarity:**
  Protection for unlimited time
- **Inrush Current Limiter**
  Peak value of 5 x I_{IN} for initial inrush currents lasting more than 50µSec.
- **Under Voltage**
  Unit shuts down when input voltage drops below 16.5± 0.5V_{DC}.
  Automatic restart when input voltage returns to nominal range.
- **Over Voltage Lock-Out**
  Unit shuts down when input steady state voltage rise above 55 ± 2V_{DC} (Can be configured for 100V)
  Automatic restart when input voltage returns to nominal range.

Output

- **Passive over voltage protection on Aux outputs**
  Zener selected at 25% ± 5% above nominal voltage, is placed across the output for passive voltage limit.
- **Active over voltage protection on VS# outputs**
  20% ± 5% above nominal voltage.
  Automatic recovery when output voltage drops below threshold.
- **Overload / Short-Circuit Protection**
  Continuous protection (10-30% above maximum current) for unlimited time (Hiccup).
  Automatic recovery when overload/short circuit removed.

General

- **Over Temperature Protection**
  Automatic shutdown at temperature of 95 ± 5°C (internal temperature)
  Automatic recovery when temperature drops below 90 ± 5°C.
  5°C Hysteresis guaranteed.

Note 1: Thresholds and protections can be modified / removed (please consult factory)

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Functions and Signals - According to VITA 62

Signal No.	Signal Name	Type	Description
1	FAIL*	Output	Indicates to other modules in the system that a failure has occurred in one of the outputs. Please refer to Figure 2 This signal is referenced to **SIGNAL RTN**.
2	SYSRESET*	Output	Indicates to other modules in the system that all outputs are within their working level. Please refer to Figure 2 This signal is referenced to **SIGNAL RTN**.
3	INHIBIT*	Input	Controls power supply outputs. This signal in conjunction with **INHIBIT** controls the outputs. Please refer to Table 1 and Figure 1 This signal is referenced to **SIGNAL RTN**.
4	ENABLE*	Input	Controls power supply outputs. This signal in conjunction with **INHIBIT** controls the outputs. Please refer to Table 1 and Figure 1 This signal is referenced to **SIGNAL RTN**.
5	GA0*, GA1	Input	Used for geographical addressing. GA1 is the most significant bit and GA0 is the least significant bit. This signal is referenced to **SIGNAL RTN**.
6	SCL, SDA	Bidirectional	I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared. This signal is referenced to **SIGNAL RTN**.
7	REF_CLK	Input	The REF_CLK signal is used to allow the power supply frequency to sync with the system frequency. This signal is referenced to **SIGNAL RTN**.
8	VOUT SENSE	Input	The SENSE is used to achieve accurate load regulations at load terminals (this is done by connecting the pins directly to the load's terminals).
9	LOAD SHARE	Bidirectional	Used for paralleling several M4065 units (optional).
10	SIGNAL RTN	Gnd	Signal ground for all signal. Internally tied to output Power ground

Table 1 – Inhibit and Enable Functionality

INHIBIT*	Low	Low	High	High
ENABLE*	Low	High	Low	High
VS1 ,VS2,VS3,±12VAux	OFF	OFF	ON	OFF
3.3V_AUX	ON	OFF	ON	OFF

Figure 1 – Inhibit and Enable Input stage

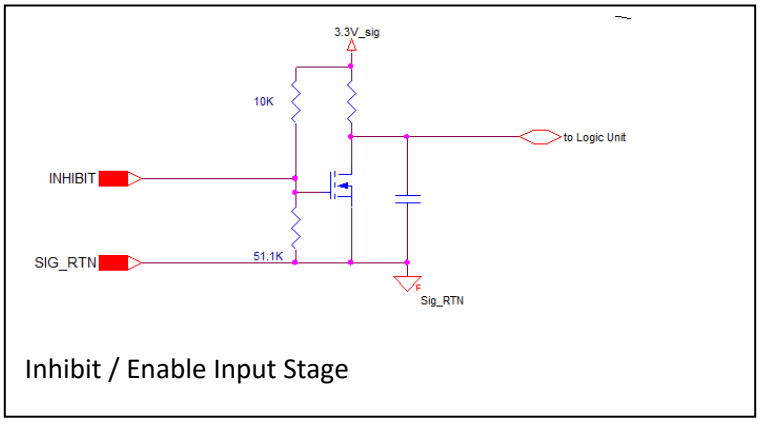
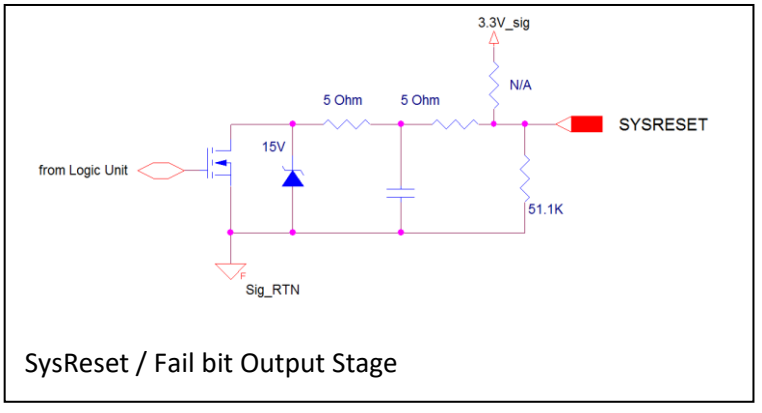


Figure 2 – SysReset and Fail Bit output stage



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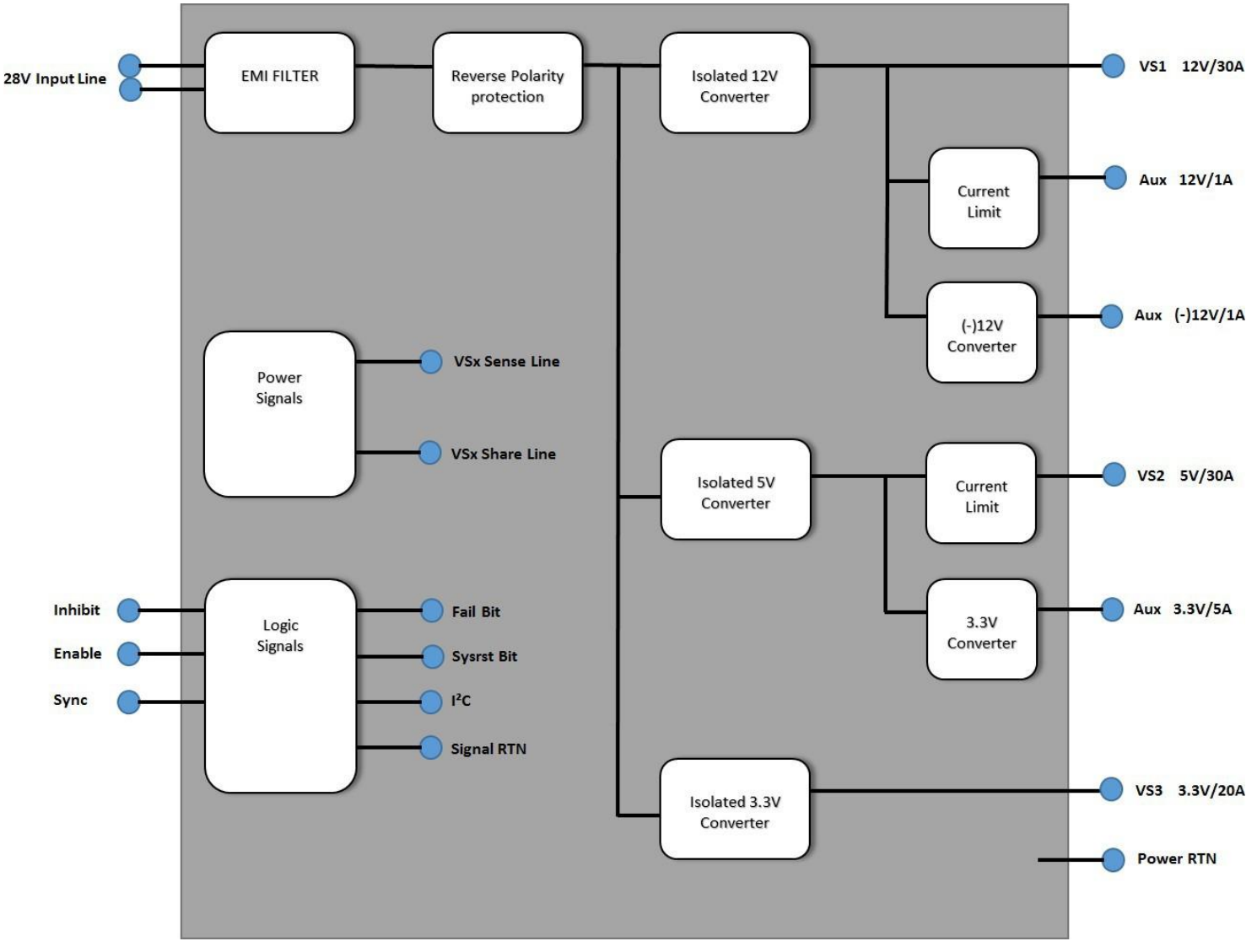
Simplified Block Diagram



Detailed Information

1. M4065 Input Voltage Operation Range.

The M4065 steady state operation voltage is 18V to 36V, continuously work up to 50V Input line.
Unit can be modified to work up to 100V or down to 12V transient and Surge.
Max Non operation Voltage 100V.

1.1 Low Line Turn-on and Turn-off Limits

To avoid Turn-on and Turn-off glitch the unit have about 2V Hysteresis. The Turn-on threshold is under 20V and turn-off below 18V.
Those limits can be adjusted, contact Factory for more information.

2. Outputs Voltage Regulation

The M4065 contains accurate internal sense lines to keep output voltage at less than 3% regulation for all Line/ Load and temperature range (see Table 2).

Output	12V/25A	5V/30A	3.3V/20A	3.3VAux/5A	12VAux/1A	(-)12VAux/1A	Notes
Voltage Range	11.85 - 12.15	4.9 - 5.1	3.28 - 3.42	3.2 - 3.4	VS1 - VS1-0.2V	(-)11.85 - (-)12.15	
Voltage Range	11.80 - 12.20	5.2 - 4.8	3.40 - 3.20	3.4 - 3.2	11.7 - 12.2	(-)11.7 - (-)12.2	Current share configuration

Table 2: Outputs voltage regulation. VIN 18V - 48V, Temperature -55C - 85C. single and parallel configuration.

2.1. Sense Lines

Sense Lines are provided for VS1, VS2 and VS3 output to compensate line voltage drop. *Sense Lines* proper connection is shown in Figure 1.
Each VSx output has its own *Sense Lines*, additional common *Sense RTN Line* is provided for all VSx Outputs (Vita 62 Standard).
Contact Factory for Sense configuration different than the Vita62 standard

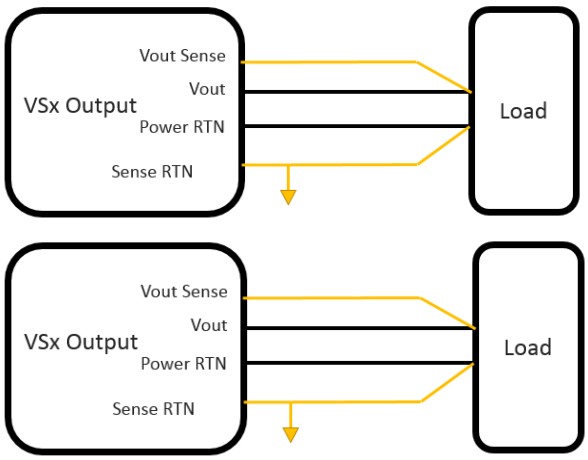


Figure 1: M4065 Sense line connection

3. Output Power

The M4065 can deliver up to 600W steady State at all temperature and input range.
Unit can support a peak power of 700W, please contact factory for more details and limitations.

Max Total Power Output	12V/30A	5V/30A	3.3V/20A	3.3VAux/5A	12VAux/1A	(-)12VAux/1A
600W	30A	30A	20A	5A	1A	1A
700W	40A	35A	20A	5A	1A	1A

Table 3: M4065-4 Max current per output

3.1. Current Sharing (Optional)

Current sharing is available for VS1, VS2 and VS3 outputs. Load share pins should be connected for Hiccup synchronization. 3.3Vaux and ±12V Aux can be safely paralleled.
To obtain a good current sharing the following steps should be taken

- Connect hiccup pins of desired outputs to guarantee simultaneously Turn-on of paralleled outputs.
- Connect Sense Line of both paralleled outputs to the same point.
- Make sure Power traces are as identical as possible for both current sharing outputs.

3.2. Mil-STD 1275E Surges (Optional for M4465 series)

Special configuration of the Unit can support up to 500W during 12V and 100V surges. Operating the unit at higher power may results in a voltage drop beyond outputs spec regulation during the surge.

Total Power Output	12V/25A[1]	5V/30A	3.3V/20A	3.3VAux/5A	12VAux/1A	(-)12VAux/1A
500W	22A	30A	20A	5A	1A	1A

Table 4: M4065 Max supported Current per output during 12V surge
Note 1: Max total current of 12V rail (12Vvs1, 12Vaux & (-) 12Vaux) should not exceed 22A in order to stay in spec regulation

Figure 2a/b shows 12VSI output during 100V and 12V surges.

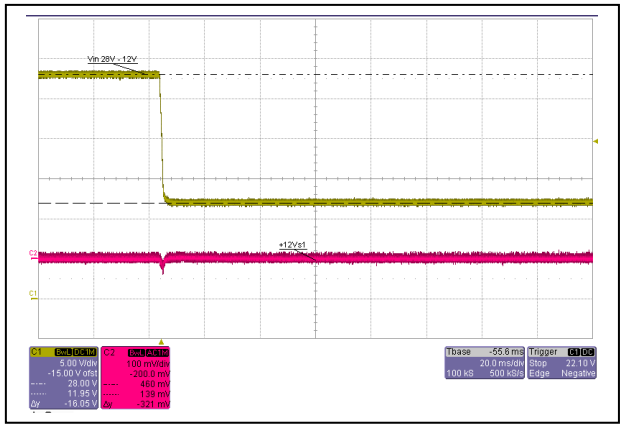


Figure 2a: VS1 during 12V Line surge

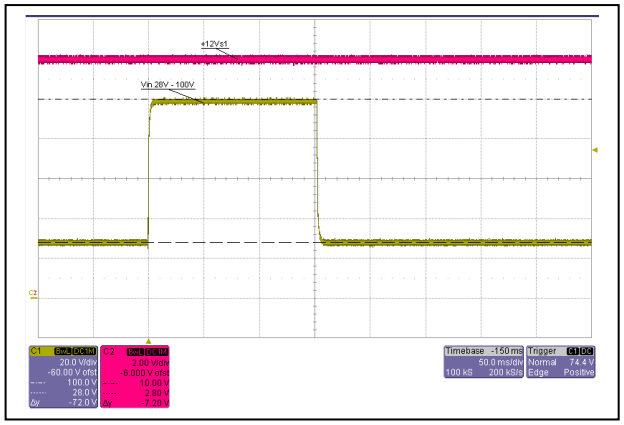


Figure 2b: VS1 during 100V Line surge

3.3. Typical Efficiency

Input Voltage	Output Power	Efficiency
28V	170W	88%
	200W	87.6%
	600W	86.1%

4. Typical EMI Tests

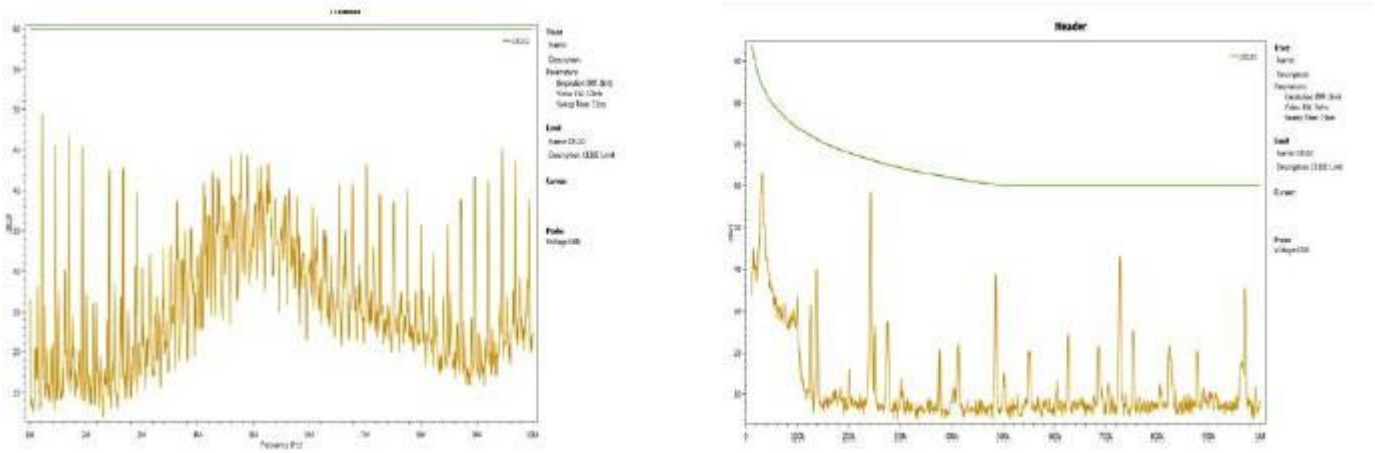


Figure 3: 28V Line, Full Load, 5UH LISN

5. IPMI Protocol

Electrical Parameters

Vcc: 3.3VDC
Pull-up: 2.2kOhm
Input capacitance: 100pf

Slave Device Addressing

- 256 address spaces
- Baud rate: 200kHz maximum
- 7 Bit Protocol
- Support Slot Addressing per VITA62
- Support Global Address 10100101 R/W

	MSB							LSB
Slot Number	A6	A5	A4	A3	A2	A1/*GA1	A0/*GA0	R/W
Slot0	0	1	0	0	0	0	0	
Slot1	0	1	0	0	0	0	1	
Slot2	0	1	0	0	0	1	0	
Slot3	0	1	0	0	0	1	1	
Global Address	1	0	1	0	1	0	1	

* Slot location is determined by GAx per Vita62.

Communications Supported

Read Command – 21Hex, deliver 64Bytes of Data. (More commands are available by request)
The communication starts when the master sends a start followed by the unit slave address, command, checksum and a stop. A second start followed by the slave address and a read will be followed by a 64 Bites response.

S	Slave Address	R/W	A	Command	A	Check sum	A	P
	A6:A0	0	0	21 Hex	0	DF Hex	0	

S	Slave Address	R/W	A	DATA	A	DATA	A	DATA	A	• • •	DATA	A	Check sum	N/A	P
	A6:A0	1	0	D7:D0	0	D7:D0	0	D7:D0	0		D7:D0	0	D7:D0	1	

Command – 21Hex read all 64 Bytes
S - Start
P- Stop

Master Transmit	Unit Transmit

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Memory Space

Response Byte #	Data Type	Meaning	Interpretation	Reading Range
0	U Integer, MSB First	Echo of Command		21 Hex
1		Reserved		00 Hex
2	S Integer, MSB First	Temperature -55C to 120C	T(C°)=+/- 7bit Dec	-55 C° to 125 C°
3		Reserved		00 Hex
4-5	U Integer, MSB First	12V VS1 Voltage	V(out) = Data· m_2	16.64
6-7	U Integer, MSB First	3.3V VS2 Voltage	V(out) = Data· m_2	16.64
8-9	U Integer, MSB First	5V VS2 Voltage	V(out) = Data· m_2	16.64
10-11	U Integer, MSB First	3.3V Aux Voltage	V(out) = Data· m_2	16.64
12-13	U Integer, MSB First	12V Aux Voltage	V(out) = Data· m_2	16.64
14-15	U Integer, MSB First	(-)12V |Aux Voltage|	V(out) = Data· m_2	16.64
16-17	U Integer, MSB First	12V VS1 Current	V(out) = Data· m_3	80A
18-19	U Integer, MSB First	3.3V VS2 Current	V(out) = Data· m_3	80A
20-21	U Integer, MSB First	5V VS2 Current	V(out) = Data· m_3	80A
22-23	U Integer, MSB First	3.3V Aux Current	V(out) = Data· m_4	n/a
24-35	U Integer, MSB First	12V Aux Current	V(out) = Data· m_4	n/a
26-27	U Integer, MSB First	(-)12V Aux Current	V(out) = Data· m_4	n/a
28-29	U Integer, MSB First	Reserved		00Hex
30-31	U Integer, MSB First	Reserved		00Hex
32-51	Character String (ASCII)	Part Number	M4065-X (Note1)	20 Characters
52-53	Decimal, MSB First	Serial Number, 2^{MSB} Dig	X,X Dec (Note2)	8 digits
54-55	Decimal, MSB First	Serial Number, 2^{LSB} Dig	X,X Dec (Note2)	
56-57	Decimal, MSB First	Date Code	Week, Year (Note3)	4 digits
58-59	Character String (ASCII)	Hardware Rev	B01 & B02 Boards (Note4)	2 Characters
60-61	Decimal, MSB First	Firmware Rev	X,X,X,X Dec (Note5)	4 digits
62	U Integer, MSB First	Reserved		AA Hex
63	U Integer, MSB First	Zero Checksum	Value required to make the sum of bytes 0 to 62 added to a multiple of 256	

Note:

$M_2 = 16.64/2^{16}-1$
$M_3 = 80/2^{16}-1$

Notes 1 to 5:

1. Part Number Example: M4065-4

Byte No'	32	33	34	35	36	37	38	39÷51
Character	M	4	0	6	5	(-)	4	0
Hex	4D	34	30	36	35	2D	34	00

2. Serial Number Example: 25

Byte No'	52		53		54		55	
Dec Number	0	0	0	0	0	0	2	5
Binary	"0000"	"0000"	"0000"	"0000"	"0000"	"0000"	"0010"	"0101"

3. Date Code Example: week 35 of 2018

Byte No'	56		57	
Dec Number	3	5	1	8
Binary	"0011"	"0101"	"0001"	"1000"

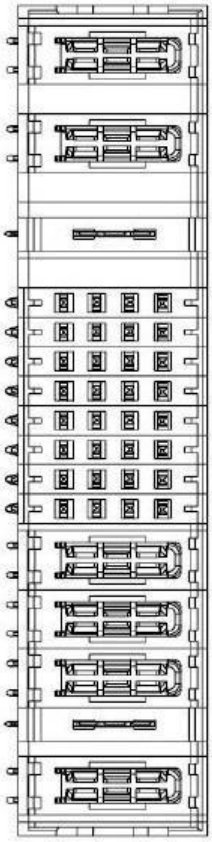
4. Hardware Rev Example: B01 Rev (-), B01 Rev A

Byte No'	58	59
Character	(-)	A
Hex	2D	41

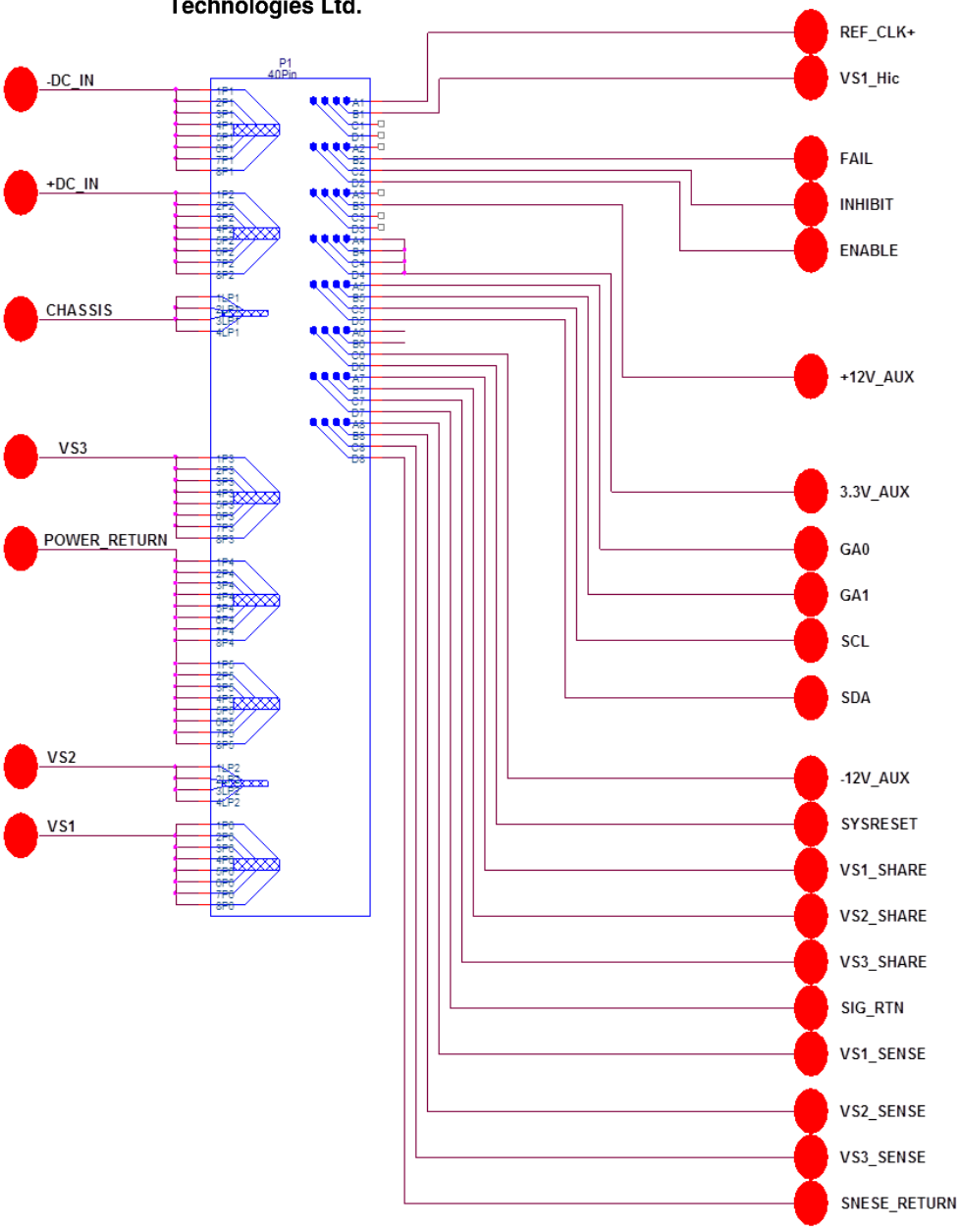
5 Firmware Rev Example: 2.1.0.0

Byte No'	60		61	
Dec Number	2	1	0	0
Binary	"0010"	"0001"	"0000"	"0000"

Pin Assignment



PART NUMBER	ROWS	POWER			SIGNAL								POWER				
		P1	P2	LP1	1	2	3	4	5	6	7	8	P3	P4	P5	LP2	P6
2ACP+ILP+32S+3HDP+ILP+1HDP	D				Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5					
6450849-7	C	TT	TT	LT	Y5	Y5	Y5	Y5	Y5	Y5	Y5	Y5	TT	TT	TT	LT	TT
	B				R5	R5	R5	R5	R5	R5	R5	R5					
	A				O5	O5	O5	O5	O5	O5	O5	O1					



Pin Number	Pin Name
P1	-DC_IN
P2	+DC_IN
LP1	CHASSIS
P3	VS3
P4	POWER_RETURN
P5	POWER_RETURN
LP2	VS2
P6	VS1
A8	VS1_SENSE
B8	VS2_SENSE
C8	VS3_SENSE
D8	SENSE_RETURN
A7	VS1_SHARE
B7	VS2_SHARE
C7	VS3_SHARE
D7	SiG_RTN
A6	N.C
B6	N.C
C6	-12V_AUX
D6	SYSRESET*
A5	GA0*
B5	GA1*
C5	SCL
D5	SDA
A4	+3.3V_AUX
B4	+3.3V_AUX
C4	+3.3V_AUX
D4	+3.3V_AUX
A3	N.C
B3	+12V_AUX
C3	N.C
D3	N.C
A2	N.C
B2	FAIL*
C2	INHIBIT*
D2	ENABLE*
A1	REF_CLK+
B1	VS1_Hic
C1	N.C
D1	N.C

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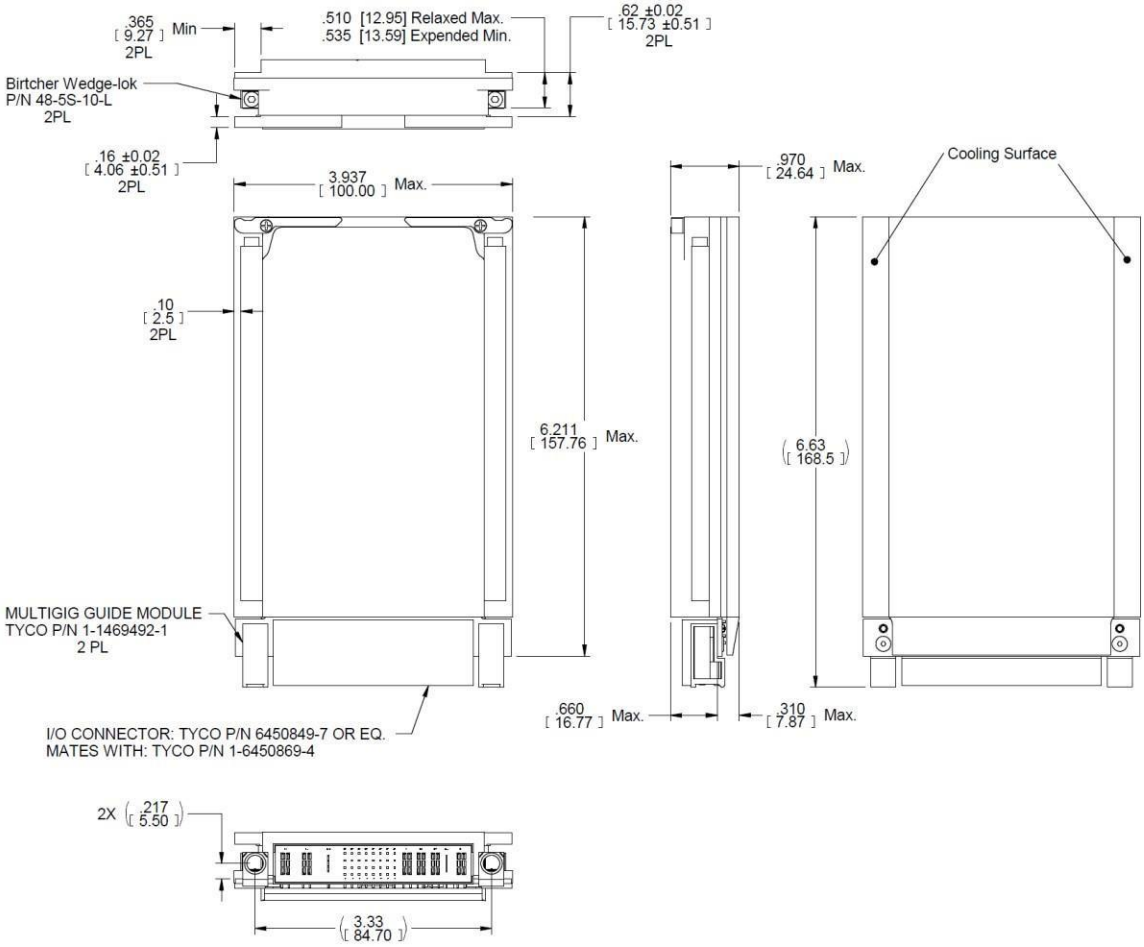
Outline Drawing



Notes

1. Dimensions are in Inches [mm]
2. Tolerance is:
   .XX ± 0.02 IN
   .XXX ± 0.008 IN
3. Weight: Approx. 796 gr
4. 3D model available